REMARKS

Claims 1, 2, 4-17, 31, and 33 remain pending in this application for which applicants seek reconsideration. Non-elected claims 5, 8-13, 15-17, and 33 remain pending in this application.

Amendment

The specification has been amended to clarify that the term "width" actually refers to the length of the first and second semiconductor regions 1, 2, i.e., along the pitch direction P1, P2. The terms "lateral width" has been included to distinguish from the "width" thereof. The lateral width refers to the dimension taken perpendicular to the pitch P1, P2.

Claims 1, 2, 6-9, 11-13, 31, and 33 have been amended to improve their clarity and form. Moreover, independent claims 1, 2, and 6 have been amended to further define that the closed loop is formed in a laminated direction of the first semiconductor regions and the second semiconductor regions, and that the lateral width of the first semiconductor regions and the second semiconductor regions forming the closed loop (at least in the straight sections in claims 1 and 6) is the same, as is clearly illustrated in the drawings. Moreover, claim 6 has been amended to recite that the first and second pitches are different. Moreover, to emphasize that the closed loop configuration, claims 1 and 6 now call for the closed loop to be formed by a plurality of straight sections and curved sections.

No new matter has been introduced.

Art Rejection

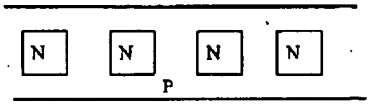
Claims 6 and 7 were rejected under 35 U.S.C. § 102(b) as anticipated by Coe (USP 4,754,310). Applicants traverse this rejection because Coe's closed loop 1) does not include a curved section, 2) does not have different pitches between the curved and straight sections, 3) does not have its alternating layers of the same lateral width, and 4) is not formed in the direction of the alternately arranged first and second semiconductor regions.

Indeed, in contrast to the examiner's assertion, Coe's closed loop is formed by a plurality of straight sections. Coe simply does not have a curved section in its closed loop, as is clearly

demonstrated by its figures. Moreover, claim 6 now recites that the first and second pitches are different. As admitted by the examiner, Coe merely has a single pitch throughout the closed loop. Claim 6 now recites that the lateral width of the first and second semiconductor regions is the same. As Coe's Fig. 1 clearly illustrates, the lateral width (distance between the two electrodes of the first and second semiconductor regions) changes according to the depth. Lastly, claim 6 more clearly recites the direction of the loop being along the lamination direction. Coe's first and second semiconductor regions alternate along a plane that is perpendicular to the closed loop direction, as previously acknowledged by the examiner. Based on these distinctions, Coe would not have anticipated or rendered obvious claims 6 and 7.

Claims 1, 2, 4-7, and 14 were rejected under 35 U.S.C. § 102(e) as anticipated by Magri (USP 6,492,691). Applicants also traverse this rejection because Margi does not disclose or teach the first and second semiconductor regions having the same lateral width, at least along the straight sections.

Referring to Magri's Figs. 6 and 8, the first semiconductor regions 34 and the second semiconductor regions 32 have different lateral widths. Although Fig. 6 appears to illustrate the lateral width of the first and second semiconductor regions 34, 32 being the same, Fig. 8 is telling. Indeed, Fig. 8 is a cross section taken along line VIII-VIII of Fig. 6, which reveals that the first semiconductor region 34 is embedded in the second semiconductor region 32. Here, the first semiconductor region 34 is an N-type source region of a MOSFET so that the second semiconductor region (P-type well) 32 has to completely surround the N-type source region 34 to isolate them from its N-type drain region 1. Otherwise, it cannot operate as a MOSFET. Accordingly, Magri's second semiconductor region 32 has to be wider and deeper than its first semiconductor region 34. That is Magri's first semiconductor regions 34 are dispersed like islands in a single P-type well 32. See below illustration. Note that the claims call for a plurality of second semiconductor regions, whereas Magri has a single second semiconductor region.



Lastly, claims 1 and 31 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kawaguchi (USP 6,297,534) in view of Bhatnagar (USP 5,710,455). Applicants also traverse this rejection because the combination, even if it were deemed proper for argument's sake, would not have taught the claimed closed looped structure formed of alternating first and second semiconductor regions.

The examiner correctly states that Kawaguchi does not disclose its alternating first and second semiconductor regions forming a closed loop. The examiner thus relies upon Bhatnagar for the proposition that forming a closed loop with the first and second semiconductor regions would have been obvious to eliminate the need for any special edge termination outside the device. Bhatnagar, in contrast to the examiner's understanding, does not disclose a closed loop formed by alternating the first and second semiconductor regions. Indeed, Bhatnagar's drift region 14 is not a loop, let alone a closed loop. Instead, the drift region 14 is merely isolated as an island. Fig. 2 illustrates a gate electrode 22 completely surrounding the drain electrode 17 to eliminate the need for any special edge termination outside the device. The gate electrode that forms a closed loop is not formed of alternating first and second semiconductor regions, but rather a single electrode. See column 6, lines 4-9. Accordingly, the combination would not have taught the claimed invention, where the closed loop comprises alternating first and second semiconductor regions.

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Conclusion

Applicants submit that the applied references do not disclose or teach the claimed loop configuration formed by alternately arranged first and second semiconductor regions having the same lateral width (at least for the straight sections). Applicants therefore urge the examiner to issue an early Notice of Allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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